ABSTRACT

The present invention provides a varactor that has increased tunability and a high quality factor Q as well as a method of fabricating the varactor. The method of the present invention can be integrated into a conventional CMOS processing scheme or into a conventional BiCMOS processing scheme. The method includes providing a structure that includes a semiconductor substrate of a first conductivity type and optionally a subcollector or isolation well (i.e., doped region) of a second conductivity type located below an upper region of the substrate, the first conductivity type is different from said second conductivity type. Next, a plurality of isolation regions are formed in the upper region of the substrate and then a well region is formed in the upper region of the substrate. In some cases, the doped region is formed at this point of the inventive process. The well region includes outer well regions of the second conductivity type and an inner well region of the first conductivity type. Each well of said well region is separated at an upper surface by an isolation region. A field effect transistor having at least a gate conductor of the first conductivity type is then formed above the inner well region.